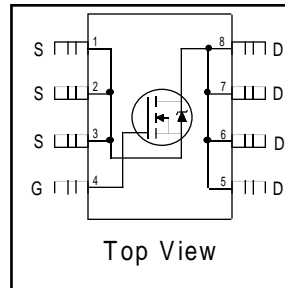


- Generation V Technology
- Ultra Low On-Resistance
- N-Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching

**Description**

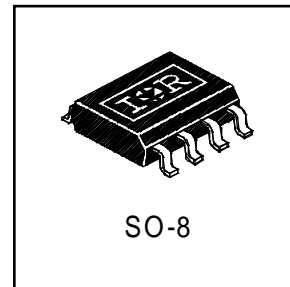
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



$V_{DSS} = 30V$

$R_{DS(on)} = 0.0135\Omega$



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8.4	
$I_{DM}$	Pulsed Drain Current ①	58	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	mW/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②	260	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to + 150	°C

**Thermal Resistance Ratings**

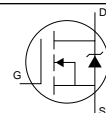
	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	—	50	°C/W

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.034	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.0135	$\Omega$	$V_{GS} = 10V, I_D = 6.6A$ ④
		—	—	0.020		$V_{GS} = 4.5V, I_D = 3.3A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	10	—	—	S	$V_{DS} = 10V, I_D = 3.7A$ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu A$	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
$Q_g$	Total Gate Charge	—	52	79	nC	$I_D = 7.3A$
$Q_{gs}$	Gate-to-Source Charge	—	6.1	9.2		$V_{DS} = 24V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	16	23		$V_{GS} = 10V$ , See Fig. 6 and 9 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	8.6	—	ns	$V_{DD} = 15V$
$t_r$	Rise Time	—	50	—		$I_D = 7.3A$
$t_{d(off)}$	Turn-Off Delay Time	—	52	—		$R_G = 6.2\Omega$
$t_f$	Fall Time	—	46	—		$R_D = 2.0\Omega$ , See Fig. 10 ④⑤
$C_{iss}$	Input Capacitance	—	1800	—	pF	$V_{DS} = 0V$
$C_{oss}$	Output Capacitance	—	680	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	240	—		$f = 1.0\text{MHz}$ , See Fig. 5⑤

## Source-Drain Ratings and Characteristics

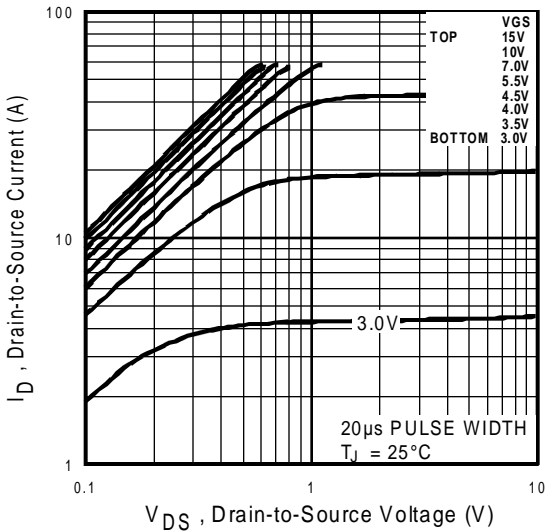
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	58		
$V_{SD}$	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 6.6A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	74	110	ns	$T_J = 25^\circ\text{C}, I_F = 7.3A$
$Q_{rr}$	Reverse Recovery Charge	—	200	300	nC	$di/dt = 100A/\mu s$ ③⑤



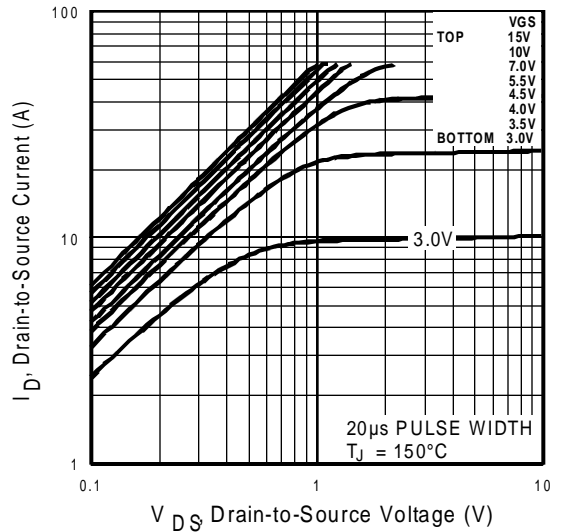
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 9.8\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 7.3A$ . (See Figure 12)
- ③  $I_{SD} \leq 7.3A$ ,  $di/dt \leq 100A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 150^\circ\text{C}$

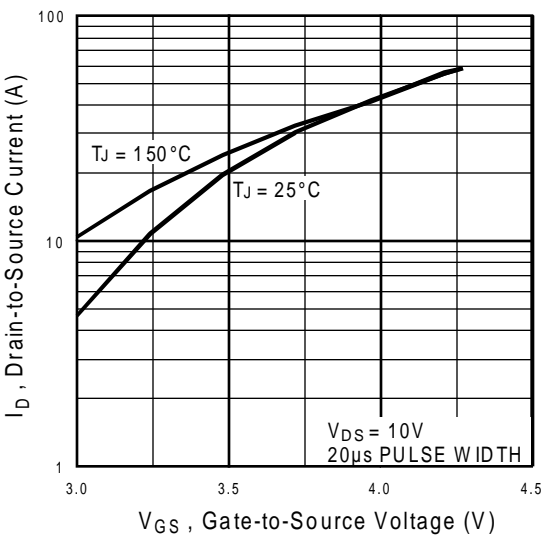
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Use IRF7413 data and test conditions
- ⑥ Surface mounted on FR-4 board,  $t \leq 10\text{sec}$ .



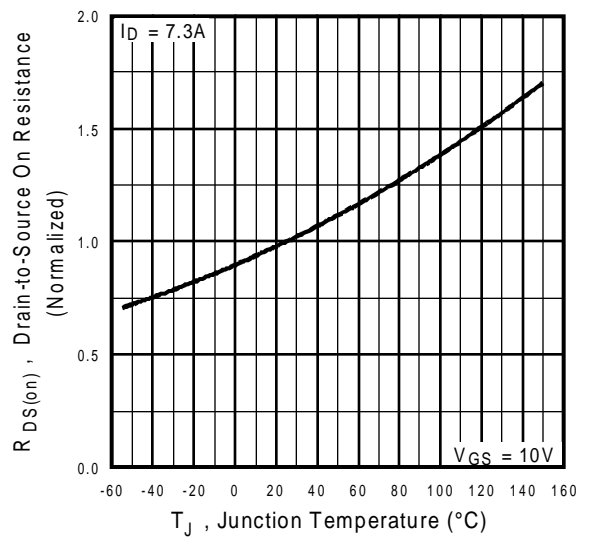
**Fig 1.** Typical Output Characteristics



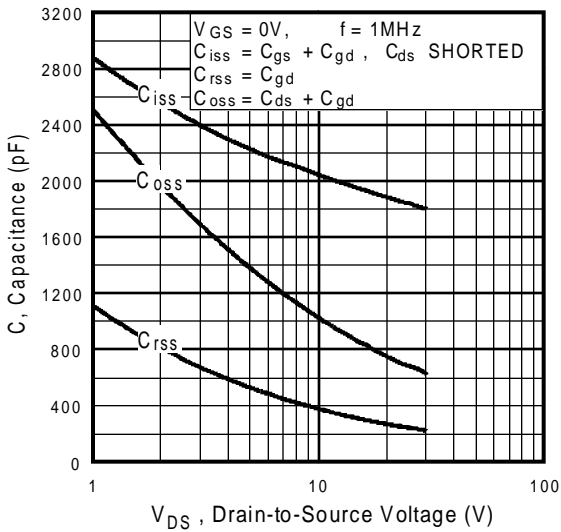
**Fig 2.** Typical Output Characteristics



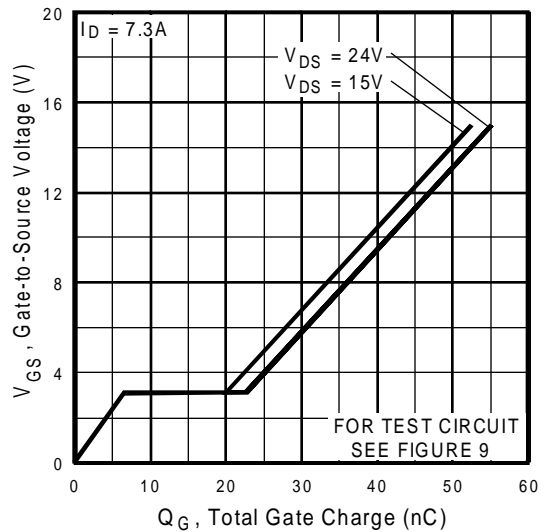
**Fig 3.** Typical Transfer Characteristics



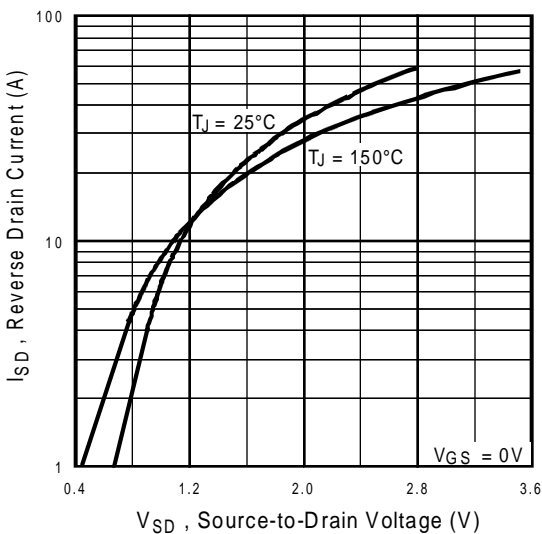
**Fig 4.** Normalized On-Resistance Vs. Temperature



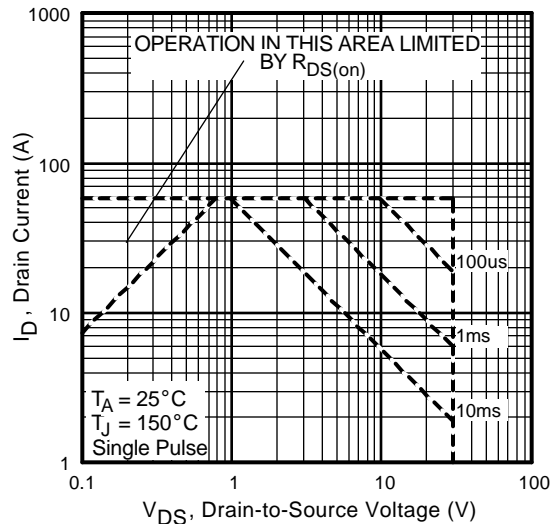
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

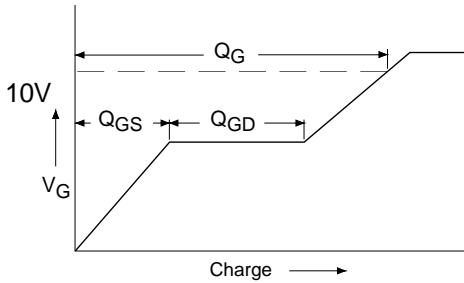


Fig 9a. Basic Gate Charge Waveform

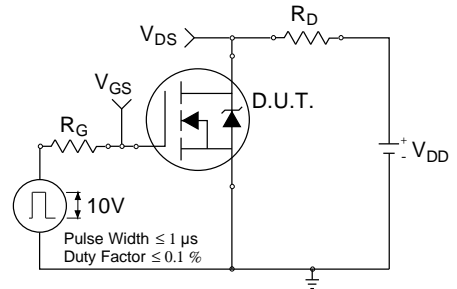


Fig 10a. Switching Time Test Circuit

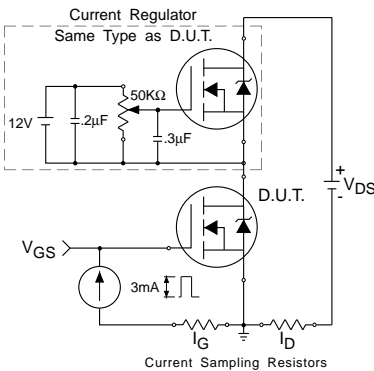


Fig 9b. Gate Charge Test Circuit

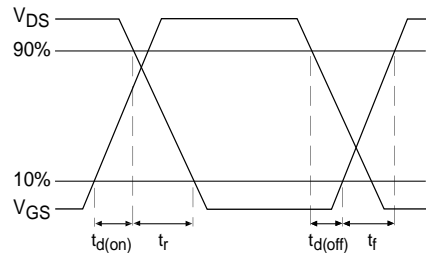


Fig 10b. Switching Time Waveforms

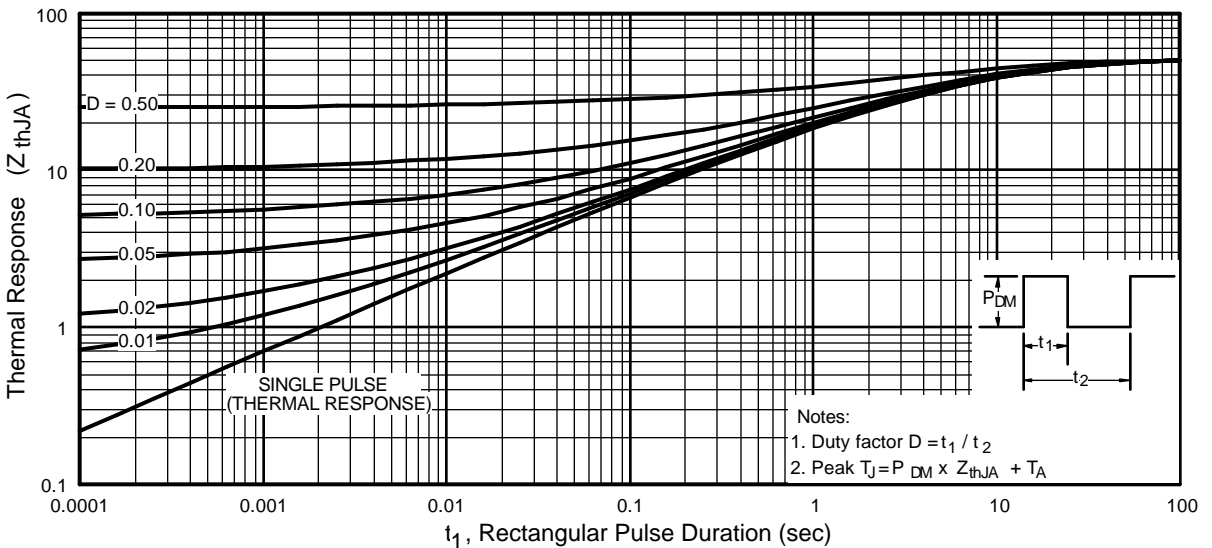
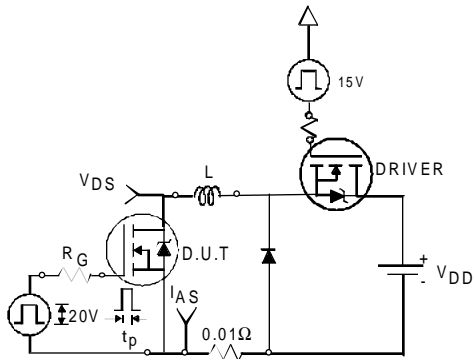
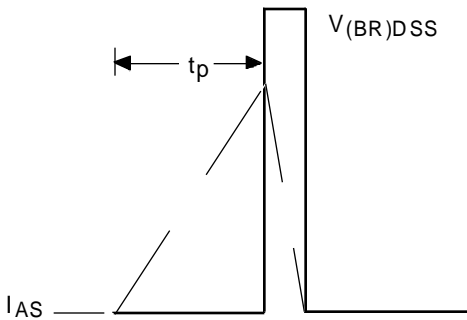


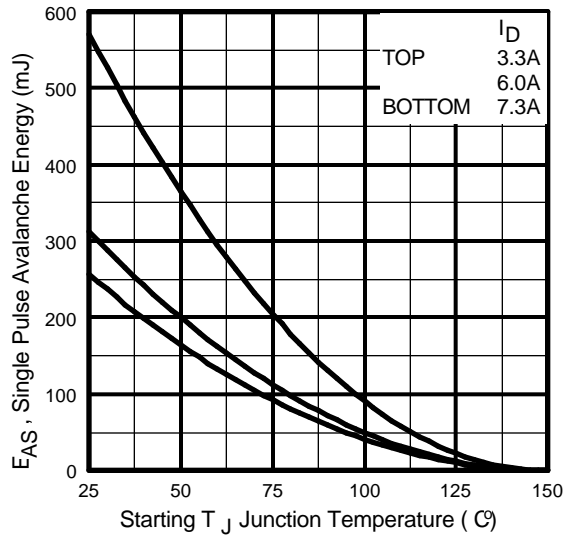
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



**Fig 12a.** Unclamped Inductive Test Circuit

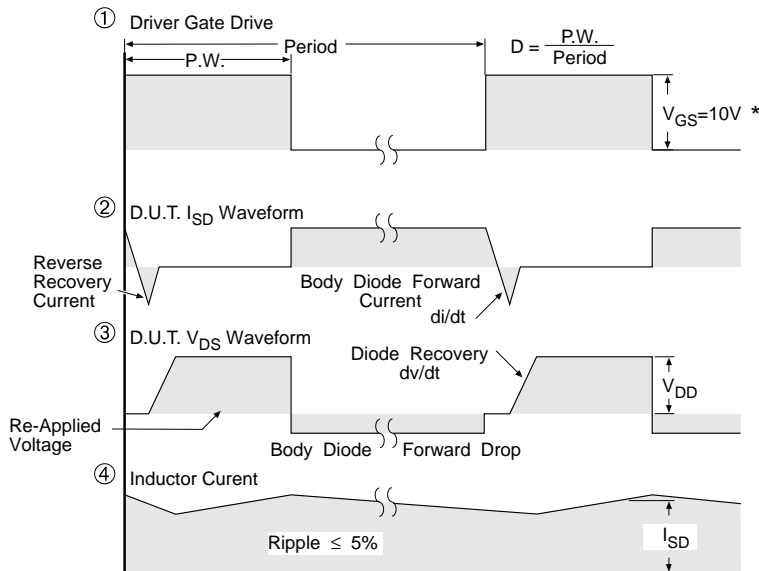
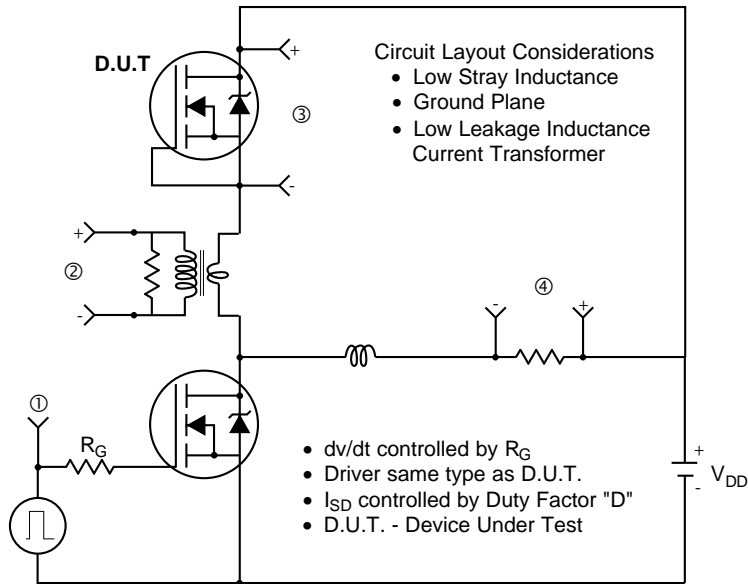


**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

## Peak Diode Recovery dv/dt Test Circuit



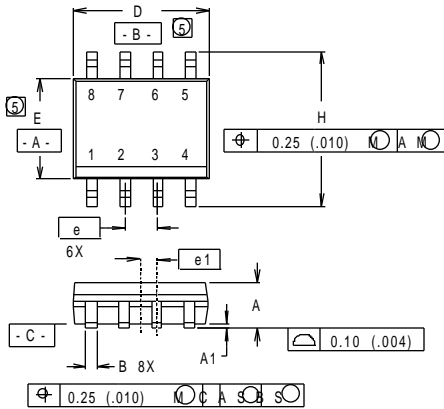
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 13.** For N-Channel HEXFETS

## Package Outline

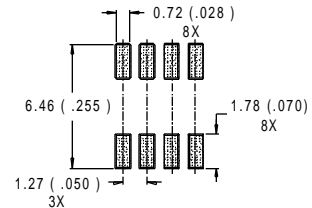
### SO8 Outline

Dimensions are shown in millimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

#### RECOMMENDED FOOTPRINT



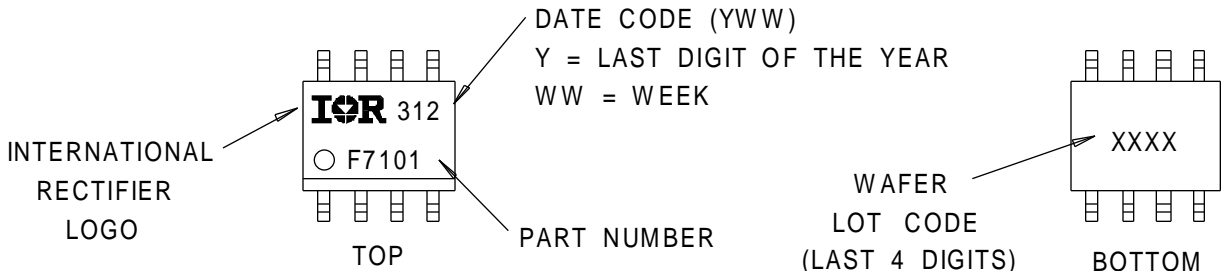
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.  
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
6. DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

## Part Marking Information

### SO8

EXAMPLE : THIS IS AN IRF7101





## Tape & Reel Information

**S08**

Dimensions are shown in millimeters (inches)

